WHAT IS CLAIMED IS:

1. A method of forming a power semiconductor device comprising the steps of:

A. providing a substrate of a first conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one trench in said epitaxial layer;

3. depositing a barrier material along the walls of said trench;

4. implanting a dopant of a second conductivity type through the barrier material into a portion of the epitaxial layer adjacent to and beneath the bottom of said trench;

5. diffusing said dopant to form a first doped layer in said epitaxial layer;

6. removing the barrier material from at least the bottom of the trench;

7. etching the trench through said first doped layer; and

8. depositing a filler material in said trench to substantially fill said trench; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.

2. The method of claim 1 further comprising the steps of:

etching the trench to a greater depth and repeating steps (B.3) – (B.6) to form a second doped layer vertically below said first doped layer; and

etching the trench through said second doped layer.

3. The method of claim 1 wherein step (C) further includes the steps of:

forming a gate conductor above a gate dielectric region;

forming first and second body regions in the epitaxial layer to define a drift

region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the first and second body regions, respectively.

4. The method of claim 1 wherein said barrier material is an oxide material.

5. The method of claim 4 wherein said oxide material is silicon dioxide.

6. The method of claim 1 wherein said epitaxial layer has a given thickness and further comprising the steps of:

D. etching the trench by an additional amount substantially equal to 1/(x+1) of said given thickness , where x is equal to or greater than two and corresponds to a prescribed number of doped layers to be formed in the voltage sustaining region;

E. repeating steps (B.3) – (B.6) to form another doped layer vertically below said first doped layer; and

F. repeating steps D-E until the prescribed number of doped layers have been formed; and

G. etching the trench through the xth layer of said doped layers.

7. The method of claim 1 wherein said material filling the trench is a dielectric material.

8. The method of claim 7 wherein said dielectric material is silicon dioxide.

9. The method of claim 7 wherein said dielectric material is silicon nitride.

10. The method of claim 1 wherein said dopant is boron.

11. The method of claim 3 wherein said body regions include deep body regions.

12. The method of claim 1, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

13. The method of claim 3, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

14. The method of claim 1 wherein said power semiconductor device is selected from the group consisting of a vertical DMOS, V-groove DMO, and a trench DMOS MOSFET, an IGBT, and a bipolar transistor.

15. A power semiconductor device made in accordance with the method of claim 1.

16. A power semiconductor device made in accordance with the method of claim 6.

17. A power semiconductor device made in accordance with the method of claim 14.

18. A power semiconductor device comprising:

a substrate of a first conductivity type;

a voltage sustaining region disposed on said substrate, said voltage sustaining region including:

an epitaxial layer having a first conductivity type;

at least one trench located in said epitaxial layer;

at least one doped layer having a dopant of a second conductivity type, said doped layer being located in said epitaxial layer adjacent a sidewall of said trench;

a filler material substantially filling said trench; and

at least one region of said second conductivity disposed over said voltage sustaining region to define a junction therebetween.

19. The device of claim 18 wherein said at least one doped layer includes a plurality of doped layers, each of said doped layers being located in a vertical column with respect to one another.

20. The device of claim 18 wherein said at least one region further includes:

a gate dielectric and a gate conductor disposed above said gate dielectric;

first and second body regions located in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type; and

first and second source regions of the first conductivity type located in the first and second body regions, respectively.

21. The device of claim 1 wherein said material filling the trench is a dielectric material.

22. The device of claim 21 wherein said dielectric material is silicon dioxide.

23. The device of claim 21 wherein said dielectric material is silicon nitride.

24. The device of claim 18 wherein said dopant is boron.

25. The device of claim 20 wherein said body regions include deep body regions.

26. The device of claim 18 wherein said trench has a circular cross-section.

27. The device of claim 26 wherein said at least one doped layer is donut-shaped.

28. The device of clam 19 wherein at least one of the plurality of doped layers is donut-shaped.

29. The device of claim 18 wherein said trench has a cross-sectional shape selected from the group consisting of a square, rectangle, octagon and a hexagon.

30. A method of forming a power semiconductor device comprising the steps of:

A. providing a substrate of a first conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one trench in said epitaxial layer;

3. depositing a barrier material along the walls of said trench;

4. implanting a dopant of a second conductivity type through the barrier material into a portion of the epitaxial layer adjacent to and beneath the bottom of said trench;

5. diffusing said dopant to form a first doped layer in said epitaxial layer;

6. removing the barrier material from at least the bottom of the trench;

7. depositing a filler material in said trench to substantially fill said trench; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.

31. The method of claim 30 further comprising the step of etching the trench through said first doped layer.

32. The method of claim 31 further comprising the steps of:

etching the trench to a greater depth and repeating steps (B.3) – (B.6) to form a second doped layer vertically below said first doped layer; and

etching the trench through said second doped layer.

33. The method of claim 30 wherein step (C) further includes the steps of:

forming a gate conductor above a gate dielectric region;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the first and second body regions, respectively.

34. The method of claim 30 wherein said barrier material is an oxide material.

35. The method of claim 34 wherein said oxide material is silicon dioxide.

36. The method of claim 31 wherein said epitaxial layer has a given thickness and further comprising the steps of:

D. etching the trench by an additional amount substantially equal to 1/(x+1) of said given thickness , where x is equal to or greater than two and corresponds to a prescribed number of doped layers to be formed in the voltage sustaining region;

E. repeating steps (B.3) – (B.6) to form another doped layer vertically below said first doped layer; and

F. repeating steps D-E until the prescribed number of doped layers have been formed; and

G. etching the trench through the xth layer of said doped layers.

37. The method of claim 30 wherein said material filling the trench is a dielectric material.

38. The method of claim 37 wherein said dielectric material is silicon dioxide.

39. The method of claim 37 wherein said dielectric material is silicon nitride.

40. The method of claim 30 wherein said dopant is boron.